Chapter 1

Introduction to Digital VLSI Systems Design

1.1 Since there are 1600x1200 pixels per image and 3 bytes per pixel, it follows that there are 1600x1200x3 bytes in the raw image. The compression is 10 and therefore, the JPEG compressed image contains 1600x1200x3/10 bytes. Two hundred such images would have 200x(1600x1200x3/10) bytes or 115.2 MB.

1.2 The picture resolution is 1024x768 pixels or 1024x768 bytes for a monochrome picture. In 4:2:0 color format, there are 6 blocks to be processed instead of 4 blocks in a monochrome picture. Therefore, the total number of bytes to be processed in 4:2:0 format is 6x(1024x768)/4 bytes. With a compression of 20, this reduces to (6x(1024x768)/4)/20 bytes of data. Since there are 30 frames per second, the number of compressed data per second is 30x(6x(1024x768)/4)/20 bytes or 8x30x(6x(1024x768)/4)/20 bits or 14155776 bits. Since the FIFO is of single bit width, the buffer memory required for storing one second is 14155776 bits.

1.3 In this format, 12 blocks are required to be processed instead of 6 blocks in 4:2:0 format. In addition, the compression is 2 times less in the 4:4:4 format. Therefore, the buffer memory required for storing one second is (12/6)x2x14155776 bits or 56623104 bits.

1.4 The FIFO size is proportionate to the picture size and is equal to (800x600/1024x768)x14155776 bits or 8640000 bits.

1.5 The total number of bytes processed in 4:2:0 format is 6x(1024x768)/4 bytes. In a second of video at 30 frames per second, there are 30x6x(1024x768)/4 bytes. Assuming one byte is processed every clock cycle, there are 30x6x(1024x768)/4 or 35389440 clock cycles in a second. Allowing some more clock cycles, the minimum clock frequency required in an FPGA implementation would be 40 MHz.

1.6 In the SVGA format, the minimum clock frequency required is proportionate to the picture size and is equal to (800x600/1024x768) x 40 MHz or 25 MHz.

1.7 There are 50x30x6x(720x525)/4 bytes to be processed in a second, where 50 is the number of channels and 30 is the frame rate. Assuming one byte is processed every clock cycle as we had done in the solution 1.5, there are 50x30x6x(720x525)/4 or 85050000 clock cycles in a second. Providing for additional cycles, we get the video encoder operating frequency of 1 GHz. The number of bits per second after the compression of 20 is (50x30x6x(720x525)/4)x8)/20 or 340200000. Hence the transmission rate over the serial channel must be better than 340 Mbps.
1.8 Since the video encoder operating frequency of 1 GHz is difficult to implement using processors right up to FPGA, ASIC is the right choice for 50 channels digital cable TV. Next best hardware in terms of throughput is the FPGA with a feasible processing speed of 100 MHz. With FPGA, we have to either scale down the number of channels to 5 or reduce the picture resolution to 256x128 pixels. Other processors would have about ten times less throughput compared to the FPGA.

1.9 Let us assume that the company used 8 nos. of analog data acquisition cards, each card housing 12 bits ADC and processing 8 analog inputs per card. Let us also assume that all the 64 analog channels are multiplexed. This means that we need 12 nos. of data bits, 6 nos. of address bits (to select one out of 64 analog channels), one bit for bank select, one no. for start conversion, one no. for end of conversion and a bit for read signal. All these add up to 22 bits and require 22 input/output (I/O) pins of FPGA to which these signals are connected. In the old FPGA board, these 22 signals would have been connected to the I/O pins of the on-board FPGA. The new FPGA board will be compatible if these signals continue to be connected to I/O pins of the FPGA. If any of these signals is not connected to I/O pin of FPGA, then the new FPGA board cannot be used without changing the signal connections in the data acquisition cards, motherboard or wire wrapper connections. In addition to this, the data acquisition speed by the new FPGA board will have to be compatible with the processing speeds of companies’ data acquisition cards. Further, the processing speed of the entire data acquisition system based on the new bought-out FPGA board will have to be the same or better than that got previously with the old FPGA board. Otherwise, real-time operation of the data acquisition system will be hampered. Also the FPGA capacity and RAM resources will have to be adequate.

1.10 The change will be acceptable provided the speed of processing is the same or better than the old FPGA board.

1.11 The new FPGA will have to be of the same package as the obsolete one if it is to be compatible. Also other on-chip resources such as RAMs and I/Os need to be adequate.

1.12 We shall assume that both the competitors used a data acquisition ASIC from another vendor and the same became obsolete. Then both the competitors are in the same plight. One solution is to develop the ASIC themselves, which would require lots of development cost as well as considerable time. A far better alternative is to use an FPGA board from a standard vendor satisfying the functional requirements described in 1.9. The next best alternative for the vendors is to fabricate the FPGA board, taking care to select a suitable FPGA holding promise of being in the market for long.

1.13 An image block is written into one of the two 64x8 bits RAMs in 8 clock cycles or 80 ns since the Clock 1 frequency is 100 MHz. In parallel to this, the DCTQ
processes all the 64 coefficients in 640 ns at Clock 1 rate. Since a block of raw image is 64x8 bits and the compression effected is 10, the compressed bits per block are 64x8/10. This compressed bit stream is processed by the serializer in (64x8/10) x 5 x 4 ns or 1024 ns since the time period of Clock 2 is 5 ns. The multiplying factor of 4 is as a result of processing in bursts of 25% duty cycle. Among the three concurrent processes, namely, image block writing (80 ns), DCTQ processing (640 ns) and VLC/serializer processing (1024 ns), the last one is the slowest and hence this determines the processing speed of the MPEG video encoder. In 4:2:0 format, there are six blocks to be processed instead of 4 in the case of monochrome image. Therefore, the processing time of a frame is (6/4) x (800x600/64) x 1024 ns or 11520000 ns or 11.52 ms, where (800x600/64) is the number of blocks in a monochrome image. This means that the frame rate achievable by the MPEG video encoder is 1/11.52 ms or 86 frames/sec.

**MPEG Video Encoder**

1.14 Before applying the video sequence, the Ready signal must be checked. If it is asserted, then one block of image is applied by applying one row consisting of 8 pixels (64 bits) at Datain [63:0] pins and the row address at WAddress [2:0] pins with Datain_valid asserted. With eight writes, one block is applied. Thereafter the Start is asserted in order to process the DCTQ. DR1_BS is toggled and filled RAM in the Dual RAM1 is read using the data Dataout and address RAddress. Concurrent to this, next input block is applied. DCTQ generates 64 coefficients at DCTQ [8:0] and its address DCTQ_Address, with their validity DCTQ_valid asserted. These coefficients are written into Dual RAM2 using Data bus and address bus Raddr. DR2_BS is toggled and filled RAM in the Dual RAM1 is read. The compressed serial bits appear at serializer output Din with Wenable asserted. The compressed bit stream is finally transmitted over a serial channel with Renable asserted.
The maximum picture size that can be processed for the frame rate of 30 per second is \((86/30) \times 800 \times 600\) using the result of solution 1.13. This works out to a maximum picture size of 1343 x 1024 pixels.

To regulate the bit stream, we must incorporate rate control. This may be done as follows. To start with, the compressed bit stream is accumulated in the 64 Kb FIFO. When it is about 90% full, the transmission over the serial channel is commenced and maintained thereafter. When the FIFO is 95 to 98% full, all the functional modules are kept in hold so that no compressed bitstream is generated. This causes the FIFO to fall since the transmission is maintained. When it falls to less than 90%, the hold is removed. This may result in increase of FIFO level until 95 to 98% full. Thus, the FIFO level will be between the two levels mentioned earlier and the transmitted bit stream may be maintained at a constant 100 MHz rate. However, there is a problem if the generated compressed bits are
low owing to high compression effected. In such conditions, the FIFO level goes below 85%. In order to prevent this fall, we may do bit stuffing of zeros at 200 MHz after processing every 16 lines. This would increase the FIFO level once again. When the FIFO level rises to 90% or over, bit stuffing is suspended and instead, the compressed bit stream generation is continued.

1. A reconfigurable video encoder can switch from one application to another dynamically and seamlessly based on user request without missing a single frame if it completes the current frame completely even after getting the user request and switches to the reconfigured standard only when the due time of a new frame arrives. For a frame rate of 30, the time interval between the commencement of one frame and the next is 33.33 ms. This can be met if processing time of a frame plus the dynamic partial reconfiguration time is less than 33.33 ms. The partial reconfiguration time for SVGA/MPEG 2 to JPEG is 220 micro second as can be seen in the second table, Partial Configuration Time. The following table shows the full configuration time for different standards. The configuration time has been arrived at from the given information, namely, the configuration stream size for an FPGA capacity of 300,000 gates is 220,000 bytes at 20 ns per byte (assuming 50 MHz frequency of configuration). For example, the total gate count for MPEG 2 is 535,000 and therefore the full configuration time is 535,000 x (220,000/300,000) x 20 ns, i.e., 7.8 ms. The partial reconfiguration time for SVGA/MPEG 2 to JPEG of 220 micro second has been computed in a similar manner, i.e., 15,000 x (220,000/300,000) x 20 ns.

<table>
<thead>
<tr>
<th>Gate Count</th>
<th>H.263</th>
<th>JPEG/MPEG 1/MPEG 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>User Interface</td>
<td>2,000</td>
<td>3,000</td>
</tr>
<tr>
<td>DCTQ</td>
<td>120,000</td>
<td>120,000</td>
</tr>
<tr>
<td>VLC</td>
<td>10,000</td>
<td>12,000</td>
</tr>
<tr>
<td>64 K/ FIFO</td>
<td>400,000</td>
<td>400,000</td>
</tr>
<tr>
<td>Total gate count</td>
<td>532,000</td>
<td>535,000</td>
</tr>
<tr>
<td>Full Configuration time in ms</td>
<td>7.8</td>
<td>7.8</td>
</tr>
</tbody>
</table>

### Partial Configuration Time

<table>
<thead>
<tr>
<th>H.263</th>
<th>JPEG/MPEG 1/MPEG 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Gate count for partial configuration (User Interface and VLC)</td>
<td>12,000</td>
</tr>
<tr>
<td>2. Partial configuration time in micro sec. (SVGA/MPEG 2 to JPEG)</td>
<td>220</td>
</tr>
</tbody>
</table>
In the dynamic configuration method, the total FPGA capacity needs to be 535,000 (in practice, 600,000). In the conventional method, the code streams of all the standards, namely, H.263, JPEG, MPEG 1/MPEG 2 will have to be resident in the FPGA. Therefore, in the conventional method, the FPGA capacity will have to be 1,602,000 gates (in practice 2,000,000), i.e., three times the dynamic configuration method. Similarly, the configuration time in the conventional method is three times (23.4 ms) the full dynamic configuration method (7.8 ms). Of course, this is a trivial factor. FPGA capacity reduction is the main advantage.

Some of the other applications of dynamic configuration are:

1. Programmable (Logic) Controller
2. PID Controller
3. Robot Controller
4. Video Scaler