From an architectural point of view, a High Performance Computing system can be described by means of a hybrid multi-level structure: at the highest level there are several systems connected among them by geographic networks (System level); an intermediate level is composed by the nodes in a single system communicating among them by means of dedicated fast networks or high performance switches (Node level); at the lowest level, finally, there are several computing elements, computing cores as well as graphic accelerators, sharing resources in a single CPU (Core level). These architecture levels have very different features and they require different algorithmic development methodologies. For such a reason, the development of algorithms and scientific software for these systems implies a suitable combination of several methodologies to deal with the different kinds of parallelism corresponding to each architectural level. The general aim is then the development of hybrid and hierarchical algorithms, able to be aware of the underlying platform. Main problems in this field are the management of large parallelism degree due to several computing units, the heterogeneity of these devices and the combination of the several kinds of parallelism in a single algorithm. These topics are mainly investigated also to gain the so called exascale performance, and, from another side, the high performance cloud computing, with regard to the so called Internet of Things and its interaction with HPC.

Starting from the Third Workshop on Models, Algorithms and Methodologies for Hybrid Parallelism in New HPC Systems, held in Krakow (Poland) in September 2015, this special issue focuses specifically on all issues related to all forms of parallelism and their combination at all levels in the emerging HPC multicomputers, with the goal of gathering the current state of knowledge in the field.

All submitted papers are subject to the same review process as those papers accepted for publication in the regular issues. The special issue seeks original papers on the range of topics related to hybrid parallelism including, but not limited to:

- Hybrid and hierarchical based parallel algorithms
- Architecture-aware parallelisation on HPC platforms
- Auto tuning techniques for heterogeneous and parallel environments
- Techniques for multi-/many-core platforms, NUMA architectures, or accelerator components
- Task scheduling and load balancing among computing elements
- Synchronization and access to shared resources
- Multilevel cache management
- Computational kernels for scientific computing and applications
- Performance and scalability models
- Tools and programming environments supporting efficient usage of multilevel parallelism.
- Resources virtualization
- Intra/Infra Virtual machines high performance communications algorithms
- Fault tolerant implementations
- Codesigning applications and HPC systems
Paper Submission and Publication

Authors are encouraged to submit high-quality, original work that has neither appeared in, nor is under consideration by, other journals. All papers will be reviewed following standard reviewing procedures for the Journal.

Paper must be prepared in accordance with the Journal guidelines: http://www.springer.com/10766.

Manuscripts must be submitted to: http://IJPP.edmgr.com, choosing "S.I. Hybrid Parallelism in new HPC Systems" as the article type.

Important Dates

Submission of Papers: February 15, 2016
First revision notification: April 30, 2016
Revised paper due: June 15, 2016
Final decision: July 31, 2016

Guest Editors

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